REMARKS

Claims 1, 8, 9, 12-14, 17-20, and 22-27 were pending in the present application. Claims 1, 8-9, 12-14, and 17-18 have been cancelled. Claim 19 has been amended. Claims 35-42 have been added. Accordingly, claims 19-20, 22-27, and 35-42 are now pending in the application.

Claim 12 stands rejected under 35 U.S.C §112, 2nd paragraph, as being indefinite. Claim 12 has been cancelled, thus the rejection is moot.

Claims 1, 8, 9, 12-14, 17-20, and 22-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gharachorloo, et al. (U.S. Patent Application Publication Number 2002/0124144) in view of Singhal, et al. (U.S. Patent Number 5,978,874), and in further view of Van Doren et al. (U.S. Patent No. 6,209,065). Applicant respectfully traverses portions of this rejection. However, in an effort to clarify the claim language, Applicant has been cancelled claim 1 and its dependent claims, and claim 35 has been added. Claim 35 has similar limitations but has clearer language.

Applicant's claim 35 recites a system comprising in pertinent part,

> wherein as part of a coherency transaction involving a coherency unit cached by the processing subsystem, the processing subsystem is configured to initiate a read-to-own transaction by sending an address packet for the coherency unit onto the address network;
>
> wherein the memory subsystem is configured to send a data packet, via the data network, indicating the read-to-own transaction to the interface in response to receiving the address packet;
>
> wherein the interface is configured to forward a read-to-own message on the inter-node network in response to receiving the data packet indicating the read-to-own transaction;
>
> wherein the additional interface is configured send an invalidating address packet on the additional address network in response to receiving

the read-to-own message, wherein in response to the additional processing subsystem having an access right to, but not an ownership responsibility for, the coherency unit, the additional processing subsystem is configured to transition its access right to the coherency unit in response to receiving the invalidating address packet, wherein the additional interface is further configured to send, via the internode network, an indication that shared copies of the coherency unit in the additional node have been invalidated;

wherein the interface is configured to delay providing to the processing subsystem another data packet including requested data on the data network until the interface receives the indication; and

wherein the processing subsystem is configured to transition **an ownership responsibility** for the coherency unit in response to receiving **a response address packet** on the address network, and to transition an access right to the coherency unit in response to the processing subsystem receiving the another data packet.

The Examiner acknowledges that Gharachorloo does not specifically teach "transition **an ownership responsibility** for the coherency unit in response to receiving **a response address packet** on the address network, and to transition an access right to the coherency unit in response to the processing subsystem receiving the another data packet," as recited in Applicant's claim 35. However, the Examiner asserts Singhal teaches the limitation at col. 27, lines 64-66. However, Singhal actually teaches

> System 30 overcomes this difficulty by distinguishing between the owner and the writer for a line. A board becomes the owner **as soon as it requests ownership**, using the ReadToOwn Address Bus packet. (*See* col. 27, lines 63-66) (Emphasis added)

Applicant submits that although Singhal discusses separating the transitions of ownership and access rights, Singhal does it differently. Clearly, Singhal is disclosing transitioning ownership rights immediately (i.e., "as soon as it requests ownership").

This is in contrast to transitioning ownership in response to the processing subsystem "receiving **a response address packet** on the address network" as recited in claim 35.

Accordingly, none of the cited references teach the above limitation. Thus Applicant submits claim 35, along with its dependent claims, patentably distinguish over the cited references for the reasons given above.

Applicant's claim 19 recites features that are similar to the features recited in claim 35. Accordingly, for at least the reasons given above, Applicant submits claim 19, along with its respective dependent claims patentably distinguishes over the cited references.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-00201/SJC.

Respectfully submitted,

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